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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/591,225	06/09/2000	David Robert Baldwin	TD-155	3467
29106	7590	09/19/2006		
GROOVER & HOLMES BOX 802889 DALLAS, TX 75380-2889			EXAMINER RICHER, AARON M	
			ART UNIT 2628	PAPER NUMBER
DATE MAILED: 09/19/2006				

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 09/591,225	<b>Applicant(s)</b> BALDWIN, DAVID ROBERT	
	<b>Examiner</b> Aaron M. Richer	<b>Art Unit</b> 2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 18 July 2006.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-5,7-10 and 12-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5,7-10 and 12-22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments filed July 18, 2006 have been fully considered but they are not persuasive.
2. As to claim 1, applicant first points out a section of Kaiser reading "without the overhead of the processor translating the addresses... and further calling OS routines to lock down these addresses in real memory" and interprets this section to read that OS routines are called and then run by a host processor. Examiner respectfully submits that this paragraph is being misinterpreted. Instead of a main processor executing OS routines, Kaiser is actually pointing out that processing is accomplished "without the overhead of... further calling OS routines..." Support for this exists at col. 2, lines 46-57 of Kaiser, which states the negatives of "pinning" or locking down an address. It is further noted that the Detailed Description of the invention (col. 4-col. 6) does not mention such a pinning or lock down operation whatsoever.
3. Applicant further argues that the host processor manages page faults as shown by col. 6, lines 3-29. Note that there are extreme page faults in Kaiser that will cause a host processor to be involved. However, there are also less-extreme page faults that will not. Examiner specifically pointed out in the previous Office Action that a graphics processor in Kaiser will "manage page faults separate from, and invisible to, the host processor as long as the page being accessed is in a second-level, or physical, memory". Col. 5, lines 45-58 describe a memory controller that if there is a "miss" (equivalent to a type of page fault) on a page of memory, a memory controller handles

address translation. Fig. 2 shows the memory of the invention directly connected to the "page table buffer" which is inside the memory controller 204. Only if "no entry is found in the system page table", is the host involved in a page fault.

This is similar to how the page faulting system claimed by applicant is described on pages 8-9 of applicant's specification. From applicant's description of an extreme page fault case: "if the faulting logical page identifies a page in the third level memory, the host does (a) (after having made the page available)". In other words, both the Kaiser reference and the applicant's invention are able to handle some, but not all, page faulting invisible to the host processor. If examiner were to interpret claim 1 as stating that "all page faulting is invisible to the host processor", it would be too narrow a read of the claim language and also inconsistent with applicant's specification.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-5, 7-10, and 12-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaiser (European Patent Publication 0 766 177) in view of Blinn (Jim Blinn's Corner "The Truth About Texture Mapping").

6. As to claim 1, Kaiser discloses a graphic accelerator unit which manages page faulting of graphics data invisibly to the host processor. Col. 3, line 50-col. 4, line 23 and col. 5, lines 37-58 describe the address translation units, in a memory controller

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with graphics engine, which manage page faults separate from, and invisible to, the host processor as long as the page being accessed is in a second-level, or physical, memory. This is similar to how the page faulting system claimed by applicant is described on pages 8-9 of applicant's specification. Col. 2, lines 1-27 explain the reasoning for making such page faults invisible to the CPU.

Kaiser discloses not specifically disclose that the graphics data being looked up is texture data. However, texture data as an example of graphics data being looked up by a graphics processor is very well-known in the art and also disclosed by Blinn. Blinn specifically discloses that the texture data, unfortunately, generates page faults when being looked up, because the texture data is so large that it cannot be fully contained by a cache or even a large RAM (p. 79, col. 1; also see further examples on p. 80-83). The advantage to using virtual memory (which causes page faults) to store texture data is to add realism by adding capacity for more texture data (p. 78, col. 1; p. 79, col. 1). It would have been obvious to one skilled in the art to modify Kaiser to also generate page faults for texture data specifically, as opposed to non-specific graphics data, in order to store more data and add realism to a scene as taught by Blinn.

7. As to claim 2, the grounds of rejection applied to claim 1 also apply to a "graphics accelerator which manages page faulting of texture data invisibly to the host processor" recited in claim 2. Claim 2 further recites that the graphics accelerator unit manages page faulting from main memory used by at least one host processor into a dedicated graphics memory, invisibly to the host processor, except when the graphics accelerator unit calls for data which has not recently been present in main memory, all of which is

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disclosed by Kaiser. Col. 5, line 37-col. 6, line 14 of Kaiser describe a TLB that is used for the graphics memory. If a page is located in physical memory, but not correctly in the page buffer, the page fault is handled by the graphics accelerator unit, invisibly to the host processor. If a page is not located in the entire system page table (physical memory) which contains pages recently present, a message is sent to the main processor to resolve the fault.

8. As to claim 3, Kaiser discloses:

at least one CPU, operatively connected to have read/write access to a main memory (fig. 2, the CPUs have access to the memory through a controller)

first memory management logic, which virtualizes said main memory with reference to at least bulk storage unit (col. 1, lines 13-45, virtual addressing on a hard disk is disclosed)

a graphics accelerator unit, comprising dedicated graphics memory, and a second memory management unit which manages texture data for said accelerator logic and performs page faulting of said texture data, invisibly to said CPU (see rejections to claims 1 and 2 and also the page buffer of figure 2 for a dedicated graphics memory).

9. As to claim 4, Kaiser discloses:

a host processor having respective physical memory associated therewith (fig. 2);

and a graphics accelerator unit having respective local memory associated therewith (fig. 2, the page buffer acts as a dedicated graphics memory), and also having a graphics memory manager (fig. 2, the controller acts as a graphics memory manager);

wherein, when said graphics accelerator unit attempts to access texture data which is in said physical memory associated with said host, said graphics memory manager fetches said texture data automatically (see the rejections to claims 1 and 2).

10. As to claim 5, Kaiser discloses a system wherein after fetching data, said graphics memory manager restarts processing (col. 6, lines 3-14; a fault causes a command to be rerun). It is not disclosed in Kaiser that texture data is fetched. Blinn, however, does disclose fetching texture data and the rationale for combining the inventions can be found in the rejection of claim 1.

11. As to claim 7, Kaiser discloses:

a host processor having host physical memory associated there with (fig. 2, the CPUs have access to the memory through a controller); and also having virtual memory management (col. 1, lines 13-45, virtual addressing on a hard disk is disclosed); and

a graphics accelerator unit having respective physical memory associated therewith (fig. 2, the page buffer acts as a memory), and also having virtual memory management (col. 5, line 37-col. 6, line 14; physical and virtual memory can be accessed);

and wherein when said graphics accelerator unit attempts to access texture data which is in said host physical memory, if said texture data is in said host physical

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memory, said graphics accelerator unit fetches said texture data from there automatically (see rejections to claims 1 and 2);

and if data is not in said host physical memory, said data is first loaded into said host physical memory, and thereafter said graphics accelerator unit fetches said data automatically from said host physical memory (col. 5, line 37-col. 6, line 14; if a page fault occurs, a host processor resolves it and resends the command, after which normal processing would occur);

It is not disclosed in Kaiser that texture data is fetched. Blinn, however, does disclose fetching texture data and the rationale for combining the inventions can be found in the rejection of claim 1.

12. As to claims 8 and 9, neither Kaiser nor Blinn explicitly teaches a graphics accelerator unit including a PCI/AGP interface, DMA controllers, SGRAM/SDRAM to which a unit has read-write access through a frame buffer and local ports, a RAMDAC, and a video stream interface. However, Official Notice has been taken that all of these are well-known modifications of a graphics processor (see MPEP 2144.03), and previous Office Actions have iterated the obviousness of such modifications as well. It would have been obvious to one skilled in the art to modify Kaiser in view of Blinn to add such modifications in order to make a graphics accelerator compatible with other computer architecture.

13. As to claims 10, 16, and 19, Kaiser discloses a host processor operatively connected to receive inputs from input devices through an interface manager chip which provides an interface to various ports and registers (col. 5, lines 2-5; also see fig. 1).



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14. As to claim 12, neither Kaiser nor Blinn explicitly teaches a bridge controller. However, Official Notice has been taken that bridge controllers are common in the art (see MPEP 2144.03), and previous Office Actions have iterated the obviousness of such a controller as well. It would have been obvious to one skilled in the art to modify Kaiser in view of Blinn to add a bridge controller to more efficiently access memory.

15. As to claim 13, Kaiser discloses a mass storage disk drive (col. 1, lines 13-45).

16. As to claim 14, the limitations of the claim also appear in claims 3 and 8, and thus claim 14 is rejected on the same grounds.

17. As to claim 15, most of the limitations are the same as claim 3 and therefore are rejected on the same grounds. The one distinct limitation in claim 15 is a recitation of a second memory management unit that manages storage in the main memory in addition to managing storage in normal memory. This is disclosed by Kaiser as well, in col. 5, line 37-col. 6, line 14, as the memory controller works with both the graphics-specific memory as well as the system memory. Kaiser does not specifically disclose texture memory, but Blinn does disclose this and the motivation for combining the inventions can be found in the rejection to claim 1.

18. As to claim 17, the limitations of the claim also appear in claims 4 and 8, and thus claim 17 is rejected on the same grounds.

19. As to claim 18, Kaiser discloses means for determining where a page is located in memory; means for updating page tables for said page; means for downloading said page; and means for restarting texture processing (col. 5, line 37-col. 6, line 14).

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20. As to claim 20, the limitations of the claim also appear in claims 7 and 8, and thus claim 20 is rejected on the same grounds.

21. As to claim 21, Kaiser discloses a system wherein an accelerator unit determines where the page is located in host physical memory to be manipulated is located; and wherein the accelerator unit determines which page out of the working set to use (col. 5, line 37-col. 6, line 14), marks this page the most recently used page, and updates the page tables for the new page and remove any reference to the page just bumped out of memory (col. 5, line 37-col. 6, line 39; a TLB is updated after pages are fetched).

22. As to claim 22, the limitations of the claim also appear in claims 3 and 21, and thus claim 22 is rejected on the same grounds.

### ***Conclusion***

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

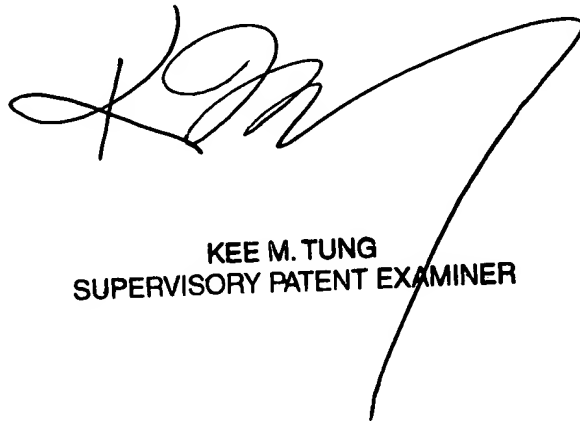
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aaron M. Richer whose telephone number is (571) 272-7790. The examiner can normally be reached on weekdays from 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AMR  
9/16/06



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